

**AMENDMENTS TO THE CLAIMS:**

This listing of the claims will replace all prior versions, and listings, of the claims in this application:

The claims are not amended, and are provided below simply for the convenience of the Examiner.

**Listing of Claims:**

1. (Original) A resonant load circuit disposed in an integrated circuit, said resonant load circuit comprising an integrated inductance in parallel with an integrated capacitance, further comprising a first integrated resistance  $R_s$  in series with one of said inductance and capacitance, and a second integrated resistance  $R_p$  in parallel with said inductance and capacitance, said first and second integrated resistances having values selected for reducing an amount of resonant load circuit Q over a plurality of instances of the integrated circuit.
2. (Original) A resonant load circuit as in claim 1, where said first integrated resistance is connected in series with said inductance.
3. (Original) A resonant load circuit as in claim 1, where said resonant load circuit forms a load in an RF low noise amplifier.
4. (Original) A resonant load circuit as in claim 1, where said resonant circuit forms a load in an RF low noise amplifier of a direct conversion receiver.
5. (Original) A resonant load circuit as in claim 1, where values for a number of units of sheet resistance for defining  $R_s$  and  $R_p$ ,  $n_s$  and  $n_p$ , respectively, are selected to obey:

$$n_p n_s = \frac{(\varpi_0 L)^2}{R_{sh0}^2},$$

where  $R_{sh0}$  is a nominal value of the sheet or unit resistance of the integrated circuit,

and where:

$$n_p = \frac{2R_L}{R_{sh0}}, \text{ and}$$

$$n_s = \frac{(\omega_0 L)^2}{2R_L R_{sh0}},$$

where  $R_L$  is a desired value of load impedance.

6. (Original) A resonant load circuit as in claim 5, where said first resistance is connected in series with said inductance, where said resonant load circuit forms a load in a balanced inductively degenerated common source low noise amplifier (LNA), and where  $R_L$  is a desired value of a parallel LNA load impedance.

7. (Original) A resonant load circuit as in claim 5, where  $R_s$  and  $R_p$  are implemented with multiple units of resistors  $R_{sh} = 100\Omega$  in order to minimize relative deviation between  $R_s$  and  $R_p$ .

8. (Original) A method to define a resonant load circuit that is disposed in an integrated circuit, said resonant load circuit comprising an integrated inductance in parallel with an integrated capacitance, comprising:

defining a first integrated resistance  $R_s$  in series with one of said inductance and capacitance; and

defining a second integrated resistance  $R_p$  in parallel with said inductance and capacitance,

where said first and second integrated resistances are defined to have values selected for reducing an amount of resonant load circuit Q over a plurality of instances of the integrated circuit.

9. (Original) A method as in claim 8, where values for a number of units of sheet resistance for defining  $R_s$  and  $R_p$ ,  $n_s$  and  $n_p$ , respectively, are selected to obey:

$$n_p n_s = \frac{(\varpi_0 L)^2}{R_{sh0}^2},$$

where  $R_{sh0}$  is a nominal value of the sheet or unit resistance of the integrated circuit,

and where:

$$n_p = \frac{2R_L}{R_{sh0}}, \text{ and}$$

$$n_s = \frac{(\varpi_0 L)^2}{2R_L R_{sh0}},$$

where  $R_L$  is a desired value of load impedance.

10. (Original) A method as in claim 9, where said first resistance is connected in series with said inductance, where said resonant load circuit forms a load in a balanced inductively degenerated common source low noise amplifier (LNA), and where  $R_L$  is a desired value of a parallel LNA load impedance.

11. (Original) A method as in claim 9, where  $R_s$  and  $R_p$  are implemented with multiple units of resistors  $R_{sh} = 100\Omega$  in order to minimize relative deviation between  $R_s$  and  $R_p$ .

12. (Original) A method as in claim 8, where said first integrated resistance is connected in series with said inductance.

13. (Original) A method as in claim 8, where said resonant load circuit forms a load in an RF low

noise amplifier.

14. (Original) A method as in claim 8, where said resonant circuit forms a load in an RF low noise amplifier of a direct conversion receiver.

15. (Original) A balanced inductively degenerated common source low noise amplifier (LNA) disposed in an integrated circuit, said LNA comprising a load impedance comprised of an integrated inductance in parallel with an integrated capacitance, further comprising a first integrated resistance  $R_s$  in series with said inductance and a second integrated resistance  $R_p$  in parallel with said inductance and capacitance, said first and second integrated resistances having values selected for reducing an amount of resonant load circuit Q over a plurality of instances of the integrated circuit.

16. (Original) A LNA as in claim 15, where said LNA forms a part of a direct conversion receiver.

17. (Original) A LNA as in claim 15, where said LNA forms a part of a RF communications device.

18. (Original) A LNA as in claim 15, where values for a number of units of sheet resistance for defining  $R_s$  and  $R_p$ ,  $n_s$  and  $n_p$ , respectively, are selected to obey:

$$n_p n_s = \frac{(\omega_0 L)^2}{R_{sh0}^2},$$

where  $R_{sh0}$  is a nominal value of the sheet or unit resistance of the integrated circuit,

and where:

$$n_p = \frac{2R_L}{R_{sh0}}, \text{ and}$$

$$n_s = \frac{(\omega_0 L)^2}{2R_L R_{sh0}},$$

where  $R_L$  is a desired value of a parallel LNA load impedance.

19. (Original) A LNA as in claim 18, where  $R_s$  and  $R_p$  are implemented with multiple units of resistors  $R_{sh} = 100\Omega$  in order to minimize relative deviation between  $R_s$  and  $R_p$ .

20. (Original) An RF transceiver comprising at least one resonant load circuit disposed in at least one integrated circuit, said resonant load circuit comprising an integrated inductance in parallel with an integrated capacitance, further comprising a first integrated resistance  $R_s$  in series with one of said inductance and capacitance, and a second integrated resistance  $R_p$  in parallel with said inductance and capacitance, said first and second integrated resistances having values selected for reducing an amount of resonant load circuit Q over a plurality of instances of the integrated circuit.

21. (Original) An RF transceiver as in claim 20, where said first integrated resistance is connected in series with said inductance.

22. (Original) An RF transceiver as in claim 20, where said at least one resonant load circuit forms a load in an RF low noise amplifier.

23. (Original) An RF transceiver as in claim 20, where said at least one resonant circuit forms a load in an RF low noise amplifier of a direct conversion receiver.

24. (Original) An RF transceiver as in claim 20, where values for a number of units of sheet resistance for defining  $R_s$  and  $R_p$ ,  $n_s$  and  $n_p$ , respectively, are selected to obey:

$$n_p n_s = \frac{(\omega_0 L)^2}{R_{sh0}^2},$$

where  $R_{sh0}$  is a nominal value of the sheet or unit resistance of the integrated circuit,

and where:

$$n_p = \frac{2R_L}{R_{sh0}}, \text{ and}$$

$$n_s = \frac{(\omega_0 L)^2}{2R_L R_{sh0}},$$

where  $R_L$  is a desired value of load impedance.

25. (Original) An RF transceiver as in claim 24, where said first resistance is connected in series with said inductance, where said at least one resonant load circuit forms a load in a balanced inductively degenerated common source low noise amplifier (LNA), and where  $R_L$  is a desired value of a parallel LNA load impedance.

26. (Original) An RF transceiver as in claim 24, where  $R_s$  and  $R_p$  are implemented with multiple units of resistors  $R_{sh} = 100\Omega$  in order to minimize relative deviation between  $R_s$  and  $R_p$ .

27. (Original) A mobile station having an RF transceiver and comprising a balanced inductively degenerated common source low noise amplifier (LNA) disposed in an RF integrated circuit, said LNA comprising a load impedance comprised of an integrated inductance in parallel with an integrated capacitance, further comprising a first integrated resistance  $R_s$  in series with said inductance and a second integrated resistance  $R_p$  in parallel with said inductance and capacitance, said first and second integrated resistances having values selected for reducing an amount of resonant load circuit Q over a plurality of instances of the RF integrated circuit.